

FUTURE of EMC Engineering

Printed Circuit Boards of the Future

BY MARK MONTROSE


Almost every electrical device has a physical structure that contains transmission lines. We call this structure a printed circuit board (PCB). There are three basic structures—rigid, flex and rigid-flex. Advances in technology mandate smaller, faster and at low cost. The company that can achieve all three elements will be successful.

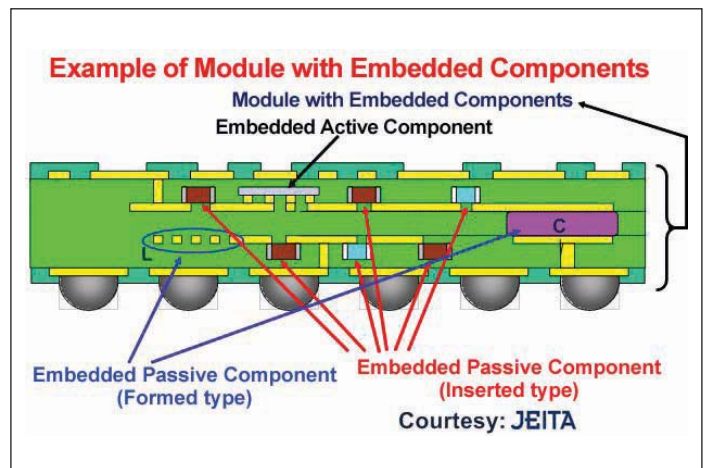
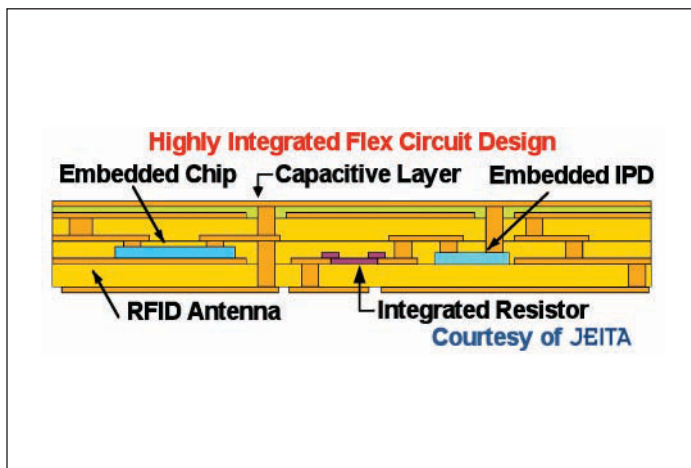
In the future, there will be a point to where the number of active and passive components that can be physically mounted onto a PCB will exceed the available real-estate of the laminate including both top and bottom layers. When this occurs the product must increase in size or features removed. This is a challenge for

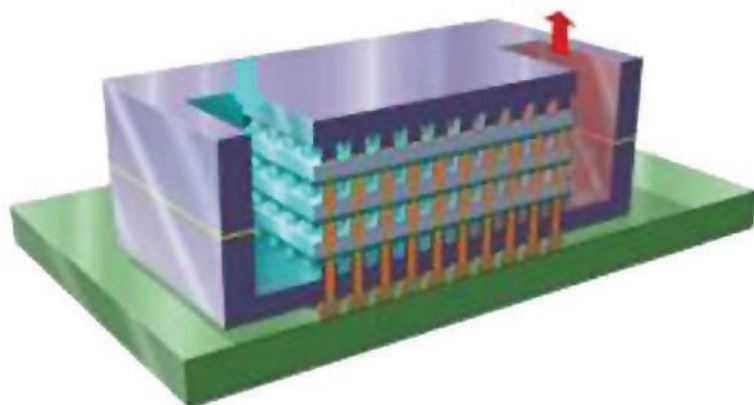
any designer. PCBs in the future may take on different forms than what we are familiar with today.

To highlight where the future of PCB technology may end up, we can expect the following will become a routine

design process. Will advances in PCB technology make more or less work for the EMC engineer?

1. Most high-technology products will be six or more layers using very thin laminates.
2. Discrete actives such as semiconductor dies, or wafers, will be embedded internal to the assembly. Embedding actives minimizes loop area inductance and allows room on both top and bottom for components and interconnects that cannot be embedded.
3. Discrete passives, such as capacitors and inductors will also be embedded along with buried capacitance layers to ensure a high quality power distribution network. Buried resistors have been around for several decades (www.ohmega.com).
4. Transmission lines will be fiber optic and not traditional copper traces. There are now PCBs that contain fiber optic traces which are made by placing glass beads in a trench within a core layer and during manufacturing melted into a fiber optic interconnect. Backplanes are also becoming fiber optic for certain high-speed applications.
5. Three dimensional components will be used with higher number of I/O pins and greater power consumption. 





3D-IC with vias and inter layer cooling channels enclosed in a sealed housing (www.PhysOrg.com)

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